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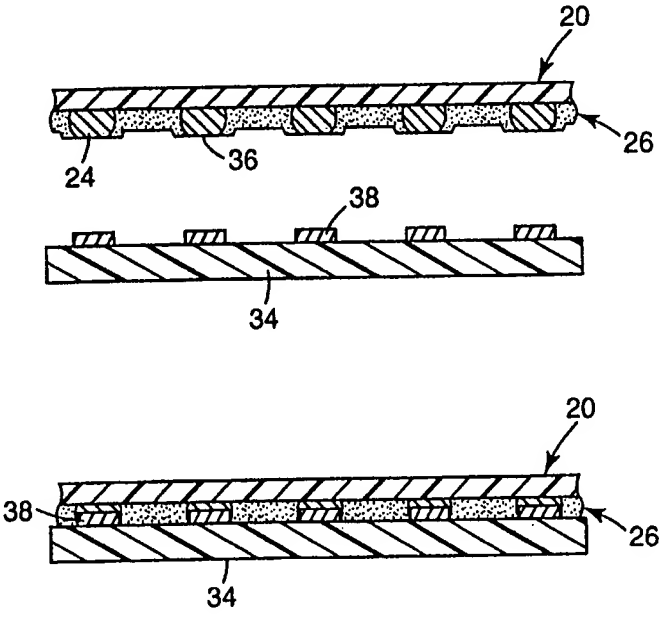

(57) Abstract

The present invention relates to a method for connecting an integrated circuit chip (20) to a circuit substrate (34). The method includes the step of pre–applying adhesive (26) directly to a bumped side of integrated circuit chip. The method also includes the step of pressing the bumped side of the integrated circuit chip, which has previously been coated with adhesive, against the circuit substrate such that the bumps (24) provide an electrical connection between the integrated circuit chip and the circuit substrate. The pre–applied adhesive

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METHODS AND APPARATUSES FOR MAKING Z-AXIS ELECTRICAL CONNECTIONS

FIELD OF THE INVENTION

The present invention relates generally methods and apparatuses for forming electrical connections. More specifically, the present invention relates to methods and apparatuses for making z-axis electrical connections between integrated circuit chips and their packaging circuits.

BACKGROUND OF THE INVENTION

The vast majority of electronic circuit assemblies in the world today utilize integrated circuit (IC) chips which have been housed in protective packages. These packages provide mechanical and sometimes thermal protection for the chips while also providing an intermediate level of interconnection between the chips and printed circuit boards. Years ago, package sizes were large compared to the size of chips. In part this was necessary because attainable feature sizes for printed circuit boards (PCB) were very large compared to those of chips. Over time, the ability to produce fine-featured circuit boards has improved and package sizes have correspondingly decreased relative to IC size. However, because of the needs to cut costs and reduce circuit size and improve performance, there has been a drive to develop circuit assembly methods which minimize the materials and processes which are required to yield a functional device.

One technique used to reduce circuit size and improve performance involves attaching IC devices directly to a substrate using perimeter or area arrays of solder balls mounted on the face of a chip. By inverting or "flipping" the chip such that the balls are placed in contact with pads on the substrate and passing the entire assembly through a solder reflow process, the IC may be metallurgically bonded to the substrate. Although flip-chip assembly technology was first pioneered over 30 years ago, it has been successfully exploited in only a few different segments of the electronics industry. The most notable examples of electronic products which have exploited flip-chip assembly include wristwatches, automotive sensors/controllers and mainframe computers. These applications are characterized by the need for either

extremely compact circuit size (watches, automotive) or by extremely high computing power per unit volume (mainframes). This underscores the simple fact that by eliminating the intermediate IC package, flip-chip assembly provides the smallest possible footprint for silicon on the circuit board.

A primary reason why flip-chip technology has not enjoyed a more widespread use is because the methodology, as it has currently been developed, is extremely process and equipment intensive. As a result, flip-chip technology is expensive to implement and provides many opportunities for problems to arise. In addition, process and performance requirements of the applications have reached the limits of current materials.

Existing flip-chip technology utilizes chips for which solder has been pre-applied to the interconnection pads. The solder is normally either a 95Pb-5Sn or a 63Sn-37Pb alloy, and it is normally reflowed to form a nearly spherical "bump" prior to final board assembly.

A typical assembly process for flip-chip assembly involves the following steps: 1) flux paste is applied to the substrate bond pads; 2) the IC is aligned and placed on the substrate while the tackiness in the flux holds the chip in place; 3) the assembly is passed through the reflow oven and the solder melts and bonds metallurgically with the substrate pads; and 4) the sample is passed through a flux cleaning operation. Flux removal has normally been done with solvent rinses. Originally it was required to use chlorinated solvents to remove the flux residues, but more recently improvements to the flux chemistry has permitted the use of more desirable solvents.

The finished flip-chip assembly must then maintain electrical continuity throughout the lifetime of the device as measured by accelerated tests such as thermal cycling and thermal shock. Mismatches of both the coefficient of thermal expansion (CTE) and the elastic modulus (E) between the silicon IC and the PCB generate high stresses in the contact joints when the circuit is passed through thermal excursions. These stresses can lead to solder joint fatigue failure after repeated temperature cycles, and this is a primary failure mechanism for flip-chip joints. This mechanism has limited the selection of substrate materials mainly to ceramic hybrid substrates such as Al_2O_3, which has high modulus and low CTE, properties similar to silicon.

Even with ceramic substrates, flip-chip assembly is limited to applications with small dice.

During the last ten to fifteen years there has been increasing interest in learning how to apply this flip-chip assembly to both larger size die and also to a broader range of printed circuit substrates. Specifically the increased wiring densities available with today's organic based substrates makes them suitable low cost substitutes for ceramic substrates. However, the relatively high CTE of organic materials has slowed the implementation of flip-chip assembly on organic substrates due to the aforementioned failure mechanism. An important breakthrough has been the development of underfill process. Underfill process uses a high modulus curable adhesive to fill the empty space between the solder balls under the chip so that the stress in the joint is shared by the adhesive and distributed more evenly across the entire interface as opposed to being concentrated at the perimeter balls. The use of an "underfill" adhesive as described above has enabled a flip-chip technology to be applied to a broader range of assemblies.

In current practice, underfill resin is applied as a liquid and is allowed to wick under the reflowed assembly. The current procedure for applying and curing underfill resins is separate from and is appended to the overall process sequence described above. After the reflow and flux removal steps, it is necessary to: pre-dry the bonded assembly, preheat the bonded assembly (to aid the wick-under), dispense resin, allow resin to wick under the die, dispense again, and then cure. Currently available underfill resins require cures of up to 2 hours at 150°C. The extra dispense steps are often needed in order to make sure that there is no entrapped air under the chip and also to provide a good fillet shape. Developing and maintaining good control over these types of material characteristics and dispensing processes is very difficult, and any imperfections will hurt the reliability of the solder joints.

Recently, an alternative approach for applying underfill resin has been pursued in which the uncured liquid resin is actually dispensed prior to the chip placement. In this case, special adhesive formulations are used that are capable of providing some degree of a fluxing action as they cure in the reflow oven. Because the resin is present on the board before the chip is placed, it is necessary to press the chip down into the resin and displace the resin from the contact sites. This approach eliminates

an extra adhesive curing step, and also eliminates the subsequent dispense and wick-under step. However, it has been shown that in order for this approach to work, the underfill resin must be unfilled. The inability to utilize fillers in the underfill resin is a constraint that substantially limits the utility of this approach. See, for example, U.S. Patent No. 5,128,746, Shi et al., High Performance Underfills for Low-Cost Flipchip Applications, Proc. 3d Int'l Symp. On Adv. Packaging Materials, March 1997; Gamota et al., Advanced Flipchip Materials: Reflowable Underfill Systems, Proc. Pac. Rim ASME Int'l Intersociety Electronic and Photonic Packaging Conf., ASME, June 1997; Johnson et al., Reflow Curable Polymer Fluxes for Flipchip Assembly, Proc. Surface Mount Int'l 1997.

The choice of chemistry for the underfill adhesive is constrained by the processing and performance requirements stated above. For best fatigue performance, it is best to choose materials that have the highest modulus and lowest CTE over the temperature range of the thermal cycling. For polymers, this means a glass transition temperature (Tg) above 170°C. By filling polymers with inorganic fillers such as SiO_2 the CTE and modulus may be brought closer to that of silicon. However, to achieve CTE of less than 30 ppm per degrees Celsius in a polymer system, a filler loading of 50% by volume or higher is typically required. Such high filler loading raises the viscosity significantly. To achieve the required balance, it is common to use epoxy resins with the lowest possible viscosity. Highly filled and cured to a high Tg, these materials are quite brittle when cured and have poor adhesion to polyimide and aluminum nitride passivation layers on the IC's. The optimization of an underfill adhesive system is, therefore, a necessary compromise between processing requirements and performance requirements. An improved flip-chip assembly process or construction which reduced or eliminated any of these materials constraints has the potential to significantly improve the reliability of flip-chip assembly through improved chemistry.

In review of the background, a reliable solder flip-chip method of IC interconnect on ceramic substrates is just beginning to be applied to organic substrates. Significant processing and materials challenges are slowing this technology in spite of strong demand from designers. The current flip-chip assembly process has too many steps, is too costly and the reliability is limited due to the

complex and conflicting materials requirements. A simplified flip-chip assembly process which reduces cost and demands from the underfill adhesive system will enable flip-chip assembly to become a more broadly attractive approach for circuit assembly.

SUMMARY OF THE INVENTION

The present invention provides a new way to simplify the flip-chip assembly process and enables the use of a broader range of materials thereby reducing assembly cost and improving interconnect reliability.

One aspect of the present invention relates to a method for connecting an integrated circuit chip to a circuit substrate. The method includes the step of pre-applying adhesive directly to a bumped side of the integrated circuit chip and removing portions of the adhesive to expose the bumps. The portions of adhesive can be removed after the adhesive application process, or can be removed during the application process. The method also includes the step of pressing the bumped side of the integrated circuit chip, which has previously been coated with adhesive, against the circuit substrate such that the bumps provide an electrical connection between the integrated circuit chip and the circuit substrate. The pre-applied adhesive on the chip forms a bond between the integrated circuit chip and the circuit substrate.

The above-described method provides numerous advantages over the prior art. For example, by applying the adhesive to the bumped IC prior to substrate attachment, encapsulation of the bumps is easier to achieve and can be more easily inspected. Also, because no wick under processes are used, the viscosity requirements for adhesive application are significantly relaxed as adhesives with viscosities on the order of about 1000 to about 30,000 poise may be used to achieve effective encapsulation. The removal of the viscosity constraint permits higher filler loading, and the use of alternative chemistries and catalysis systems. Such extra formulation latitude has the potential to enable higher reliability assemblies through improved adhesive material properties. Additionally, the above-described method offers the potential for fluxless attach due to the scrubbing action of the bumps as they deform in the bonding process.

Another aspect of the present invention relates to a method for preparing integrated circuit chips for assembly. The method includes the step of providing a wafer including a bumped side having a plurality of conductive bumps. The method also includes the steps of applying adhesive to the bumped side of the wafer, and dicing the wafer into individual integrated circuit chips. Because the adhesive is deposited at the wafer level, no dispensing, wicking, or damming are required. Additionally, with the use of faster curatives, post curing may be eliminated.

A further aspect of the present invention relates to an integrated circuit chip. The integrated circuit chip includes a bumped side having a plurality of conductive bumps. The chip also includes a layer of adhesive that covers the bumped side. The bumps have exposed contact regions that are substantially uncovered by the adhesive layer. The adhesive layer protects the bumped wafer during handling to increase yields. The exposed contact regions facilitate providing an electrical connection with a circuit substrate.

Still another aspect of the present invention relates to a conductive tape including an adhesive layer having a top surface and a bottom surface. The tape also includes a plurality of conductive particles disposed within the adhesive layer. At least one of the particles has an exposed top contact region at the top surface of the adhesive layer, and an exposed bottom contact region at the bottom surface of the adhesive layer.

One further aspect of the present invention relates to a method for providing an electrical connection between first and second electrical components. The method includes the step of providing a conductive tape having an adhesive layer including a top surface opposite a bottom surface and a plurality of conductive particles disposed within the adhesive layer. Each of the particles extends across a thickness of the adhesive layer and includes an exposed top contact region located at the top surface of the adhesive layer, and an exposed bottom contact region located at the bottom surface of the adhesive layer. The method also includes the step of pressing the conductive tape between the first and second electrical components.

An additional aspect of the present invention relates to a method for making a

conductive tape. The method includes the step of applying adhesive to a plurality of conductive particles, and removing portions of the adhesive that overcoat the conductive particles such that exposed contact regions of the conductive particles are generated.

A variety of additional advantages of the invention will be set forth in part in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The advantages of the invention will be realized and attained by means of the elements and combinations particularly pointed out in the claims. It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate several embodiments of the invention and together with the description, serve to explain the principles of the invention. A brief description of the drawings is as follows:

Figs. 1A-1C illustrate a method for preparing an IC chip for connection to a circuit substrate;

Figs. 2A-2B illustrate a method for connecting the prepared IC chip of Fig. 1C to a circuit substrate;

Figs. 3A-3B are micrographs of an IC chip processed via the method of Figs. 1A-1C, Fig. 3A shows the chip prior to abrasion and Fig. 3B shows the chip after abrasion;

Figs. 4A-4C illustrate an alternative method for preparing an IC chip for connection to a circuit substrate;

Figs. 5A-5B are micrographs of an IC chip processed via the method of Figs. 4A-4C, Fig. 5A shows the chip prior to abrasion and Fig. 5B shows the chip after abrasion;

Fig. 6A is a cross-sectional micrograph of an IC chip connected to a circuit substrate, the IC chip was not subjected to an abrasion step prior to connection;

Fig. 6B is a cross-sectional micrograph of an IC chip connected to a circuit substrate, the IC chip was subjected to an abrasion step prior to connection;

Figs. 7A and 7B illustrate a method for making a conductive tape; and

Figs. 8A and 8B illustrate a method for making an electrical connection using the conductive tape of Figs. 7A and 7B; and

Figs. 9A-9D illustrate a method for encapsulating bumps on wafer integrated circuits.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to exemplary embodiments of the present invention which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

The present invention provides an alternate means for applying underfill adhesive resin to an IC chips. In this case, underfill resin is applied to the bumped sides of IC chips, preferably at wafer level, before the chips have been bonded to an interconnect substrate such as a printed circuit board (PCB). The resin may be applied by techniques such as laminating a film material or by liquid coating. In contrast to traditional underfill methods that rely on wicking to cover the hidden surface, the present invention allows resin to be directly coated on the entire exposed surface/face of the IC chips. Consequently, the problems with entrapped air or incomplete filling typically associated with the traditional underfill are eliminated. With the present method, underfill resin coverage and thickness can be controlled to ensure uniformity. Because the wick-under process is eliminated, rheological requirements of the uncured resin are relaxed. This in turn can permit the use of alternative chemistries and higher filler loading to attain better mechanical properties after cure.

After the chips have been coated with the adhesive resin, or during the coating process itself, portions of the adhesive resin are removed to expose the tops of the solder bumps. For example, a mechanical process can be used to remove the previously applied adhesive from the tops of the bumps. Exemplary processes include rubbing the adhesive with an abrasive material, scraping the adhesive with a

knife edge, or compressing the adhesive to thin and eventually crack or otherwise displace the adhesive material from the tops of the bumps. The above-described adhesive removal step is important because to achieve good metal-to-metal contact between the solder bumps and the interconnect substrate prior to the reflow step, the top surfaces of the bumps should preferably be at least partially exposed. The adhesive removal and bump exposing step also function to remove oxide films from the bumps that were formed during their initial reflow. Immediately after the bump exposure operation has been completed, a film or other type of protective cover may be applied to the wafer/chips to protect the adhesive and the exposed bumps.

After the protective film or cover has been applied to the chips, the wafer forming the chips is diced into a plurality of discrete chips. Following wafer dicing and removal of the protective film, a selected IC chip can be aligned and pre-attached to the interconnect substrate with heat and pressure. During this pre-attachment step, the solder bumps of the chip are deformed slightly in order to further ensure both good metal to metal contact between the IC and the interconnect substrate as well as good wetting of the adhesive to the substrate. Specifically the bump deformation accommodates the stand off of the IC from the substrate and allows the adhesive to be brought down to contact and fully wet the substrate surface thereby completely filling the cavity under the chip. In addition, the collapse of the bumps causes the surface oxides on the solder bumps to crack and open exposing fresh solder which is then smeared across the substrate pads forming a good metallurgical bond.

When the resin-coated IC chip is bonded to the interconnect substrate, the pre-applied adhesive forms and maintains a mechanical bond between the chip and the substrate significantly reducing the stress in the solder joints. Depending on the application, the solder joints may be formed without flux and still form reliable interconnects. In this case, the adhesive serves to affix the IC to the board prior to reflow instead of a flux paste. The solder reflow process can also serve to partially or even fully cure the underfill resin, which can possibly eliminate the need for an additional post cure.

Figs. 1A-1C show an exemplary process, in accordance with the principles of the present invention, for preparing an IC chip for electrical connection to a circuit substrate. Fig. 1A shows an IC chip 20 or wafer having a passivation surface 22 on

which a plurality of conductive bumps 24, such as solder bumps, are disposed. The bumps 24 can be made of a variety of known conductive materials. Exemplary materials include meltable solid metals, gold, conductive slurries, conductive polymers, electroless nickel, and electroless gold.

The bumps 24 are preferably deposited on input/output pads of the chip 20 and protrude or project outward from the passivation surface 22 of the chip 20. The bumped side of the chip 20 has been covered with a layer of adhesive material 26 such as adhesive film or adhesive solution. The adhesive can be deposited or applied to the bumped side of the chip by any number of known techniques. For example, the adhesive can be coated as a hot melt, coated from solution, or bonded as a film in a lamination process.

The adhesive material 26 fills the volume around the bumps 24 and protects the bumps 24 during handling prior to assembly. As shown in Fig. 1A, the adhesive material 20 has a thickness which is less than the heights of the bumps 24. As a result, the exposed surface of the adhesive 26 has a plurality of adhesive protuberances 28 that correspond to the bumps 24. The protuberances 28 cover the bumps 24 and project outward from a substantially flat primary adhesive surface 30 that is located between the bumps 24. If the adhesive is applied as a liquid, the liquid is preferably b-stage cured or dried to form an adhesive film.

To ensure a better electrical connection with a substrate, it is preferred to at least partially remove the adhesive protuberances 28 that cover the bumps 24. As shown in Fig. 1B, an abrasion process is employed to remove the adhesive material located on top of the bumps 24 exposing the conductive bumps 24 for better electrical connection with a packaging substrate. In the abrasion process, an abrasive material 32 such as sandpaper, micro abrasive, abrasive pads available from 3M Company, St. Paul, MN under the trade designation Scotch Bright, a cloth, a scraping blade or a coating knife is brought in contact with the adhesive protuberances 28 that cover the bumps 24 such that the bumps 24 are exposed for electrical conduction. Because the protuberances project above the average adhesive height on the chip 20, such protuberances become pressure focal points that receive the most abrasion or cutting. Fig. 1C shows the chip 20 after the bumps have been exposed via abrasion. Once the

bumps have been exposed, a film, tape or other type of protective cover may be applied to the chip 20 to protect the adhesive 26 and the exposed bumps 24.

A variety of techniques can be used to expose the conductive bumps 24. If the adhesive is coated as a liquid, a scraper or knife edge can be used to remove adhesive from the bumps during the coating process. For example, the knife could be used to spread the adhesive and simultaneously remove portions of the adhesive from over the bumps 24. Alternatively, the bumps 24 could be exposed via abrasion after the liquid adhesive has hardened. Furthermore, the adhesive could be applied as a film with portions of the film being removed by an abrasion process.

As shown in Fig. 1C, each bump 24 extends completely across the adhesive layer 26. In this manner, the height of each abraded bump 24 is roughly equal to or higher than the thickness of at least portions of the adhesive layer 26. Additionally, the exposed regions 36 of the bumps 24 are slightly raised with respect to the primary adhesive surface 30.

Figs. 2A and 2B illustrate a method for electrically connecting the prepared chip 20 to a circuit substrate 34 such as a packaging circuit. To connect the chip 20 to the circuit substrate 34, exposed regions 36 of the bumps 24 are aligned with circuit pads 38 of the circuit substrate 34. Next, the chip 20 is pressed against the circuit substrate 34 with sufficient force to generate electrical contact between the bumps 24 and the circuit pads 38, and to cause the adhesive 26 to wet and fill around the bumps 24 and circuit substrate 34.

It is preferred for the bumps 24 to deform during the bonding process. By deforming the bumps 24, standoff between the chip 20 and the substrate 34 is reduced and the adhesive 26 is caused to fully wet and encapsulate the substrate circuit topography expelling entrapped air. The adhesive 26 may be cured during the bonding process or in a separate bake cure at a later time. Once cured, the adhesive 26 provides the mechanical bond between the IC chip 20 and substrate 34, redistributes the stresses at the solder joints and encapsulates the bumps 24 protecting them from the environment.

In an experimental example that illustrates the above-described aspects of the present invention, an IC chip manufactured by Flipchip Technology was utilized. Solder bumps having 4 mil diameters were located on the perimeter of the chip. An

adhesive manufactured by DuPont, with a trade name of Pyralux LF, was used to overcoat the bumps. Specifically, a 3 mil thick layer of adhesive was placed on the bumped chip surface by pressing the adhesive to the chip that was heated to 100°C on a hot plate. Fig. 3A is a micrograph of the chip after having been coated with adhesive. The 4 mil tall bumps were higher than the thickness of the adhesive, so there was substantial protrusion of these bumps above the primary adhesive surface on the chip surface. An Imperial Lapping Film micro abrasive manufactured by 3M Corporation was used to remove the adhesive from the tops of the bumps so as to expose the bumps. Fig. 3B is a micrograph the chip after the bumps have been exposed via abrasion. Inspections of the abraded parts found no evidence of abraded conductive material on the processed parts. The abraded adhesive and bump materials were apparently carried away by the abrasive film.

Figs. 4A-4C illustrate another process, in accordance with the principles of the present invention, for preparing an IC chip for connection to a circuit substrate. It will be appreciated that the process of Figs. 4A-4C has aspects that are similar to the process of Figs. 3A-3C. For example, Fig. 4A shows an IC chip 120 including a plurality of conductive bumps 124 deposited on a passivation surface 122 of the chip 120. The bumped side of the chip 120 is covered with a layer of adhesive material 126 having a thickness equal to or greater than the heights of the bumps 124. The adhesive material 126 covers the bumps 124 and has an exposed primary surface 130 that is substantially parallel to the passivation surface 122.

As shown in Fig. 4B, a cutting or abrasion process is employed to remove the adhesive material on top of the bumps 124 exposing the conductive bumps 124 for better electrical connection with a packaging substrate. In the abrasion process, an abrasive material 132 is used to burnish the entire primary surface 130 of the adhesive 126 such that the bumps 124 are exposed for electrical conduction. Fig. 4C shows the chip 120 after the bumps have been exposed via abrasion. Once the bumps have been exposed, a film, tape or other type of protective cover may be applied to the chip 120 to protect the adhesive 126 and the exposed bumps 124.

As shown in Fig. 4C, each bump 124 extends completely across the thickness of the adhesive layer 126. In this manner, the height of each abraded bump 124 is roughly equal to the thickness of at least portions of the adhesive layer 126.

Additionally, the exposed regions 36 of the bumps 24 are substantially flush with respect to the primary adhesive surface 30. It will be appreciated that the chip 120 can be connected to a circuit substrate in substantially the same manner previously described with respect to Figs. 2A and 2B.

Fig. 5A is a micrograph of an exemplary chip having bumps which have been coated with adhesive in the same manner the chip 120 of Fig. 4A. Additionally, Fig. 5B is a micrograph of the chip of Fig. 5A after portions of the adhesive have been abraded to expose the conductive bumps.

With respect to the above-described embodiments, if the adhesive coating has low flow characteristics during bonding, non-polished bumps may not be able to push through the adhesive to make contact with the bonding pads. Fig. 6A shows a cross-sectional image of a non-abraded chip bonded to a FR4 board using Pyralux, a no-flow adhesive manufactured by DuPont. The cross-sectional photo shows that the bumps are not in contact with the substrate because the adhesive is thick and covering the bumps. Fig. 6B shows a cross-sectional image of a polished/abraded chip bonded to a FR4 board using Pyralux. In contrast to the chip of Fig. 6A, the cross-section photo of Fig. 6B shows that the bumps are in contact with the substrate because the polishing process was used to remove the extra adhesive from the bump tops.

If the adhesive coating flows significantly, the bumps will push through the adhesive somewhat during bonding. However, the adhesive 126 can get trapped under the bump, thereby preventing good metallurgical bond formation. Consequently, even when high flow adhesives are utilized, it is still typically preferred to abrade the adhesives.

Figs. 7A-7B show another aspect of the present invention which relates to a method for making a z-axis conductive tape. The method includes the step of providing an array of conductive particles 210. An exemplary size distribution for the particles is from 20-75 micrometers. The method also includes the step of coating the particles 210 with a layer of adhesive 214 as shown in Fig. 7A. The adhesive 214 can be applied to the particles 210 by a variety of techniques. For example, the adhesive can be coated as a hot melt, coated from solution, pressed as a film upon the particles 210, or bonded as a film in a lamination process. Additionally, the particles can be

mixed within an adhesive suspension which is spread to form a layer or film of adhesive having a plurality of coated particles contained therein.

The adhesive 214 has a primary thickness t that is less than the size of the particles 210. As a result, the adhesive 214 has a top surface 216 having a plurality of humps or top protuberances 218 that correspond to the particles 210. The adhesive 214 also includes a bottom surface 217 having a plurality of bottom humps or protuberances 219 that correspond to the particles 210. Of course, in alternative embodiments of the present invention, the adhesive may have a primary thickness equal to or greater than the size of the particles. In such an embodiment, the adhesive would preferably define substantially flat top and bottom surfaces.

After the adhesive 214 has been applied to the particles 210, at least portions of the top protuberances 218 are removed such that top contact regions 220 of the particles 210 are exposed. Similarly, at least portions of the bottom protuberances 219 are removed such that bottom contact regions 224 of the particles 210 are exposed. The particles 210 can be exposed by techniques such as burnishing or polishing the top and bottom surfaces 216 and 217 of the adhesive 214 with an abrasive material.

In certain embodiments of the present invention, the particles 210 can initially be supported on a release liner (not shown) while adhesive is applied to the particles 210. In such an embodiment, after the particles 210 have been covered with the adhesive 214 and the top contact regions 220 have been exposed by techniques such as abrasion, the liner is removed from the back or bottom side 217 of the adhesive 214 allowing the bottom side 217 of the adhesive to be processed.

Fig. 7B shows the adhesive 214 after the top and bottom contact regions 220 and 224 have been exposed. The product depicted in Fig. 7B comprises a strip of conductive tape 226 suitable for providing z-axis electrical connections. The particles 210 of the tape 226 have sizes substantially equal to or greater than the thickness of the adhesive 214. As a result, each particle 210 extends completely across the thickness of the adhesive 214. A protective film or cover can be used to protect the exposed top and bottom contact regions 220 and 224 until the tape 226 is actually used to provide an electrical connection.

Figs. 8A and 8B show a method of providing a z-axis connection between first and second electrical components 228 and 230 using the conductive tape 226. As shown in Fig. 8A, the conductive tape 226 is positioned between conducting pads 232 of the electrical components 228 and 230. Next, as shown in Fig. 8B, the tape 226 is pressed between the electrical components 228 and 230 with sufficient force to generate electrical contact between the particles 210 and the circuit pads 232. While the tape 226 is pressed, the tape 226 is also heated such that the adhesive 214 wets and fills around the particles 210, and forms a bond between the electrical components 228 and 230. The adhesive can be cured during the bonding process or in a separate bake cure at a later time.

Figs. 9A-9D illustrate an exemplary method for manufacturing integrated circuit chips in accordance with the principles of the present invention. Fig. 9A shows a wafer 320 having a passivation surface 322 on which a plurality of conductive bumps 324 are disposed. An adhesive film 326 with a protective backing 328 is located adjacent to the passivation surface 322.

Fig. 9B shows the adhesive film 326 being pressed against the passivation surface 322 of the wafer 320. As the adhesive film 326 is pressed against the wafer 320, the adhesive 326 covers the bumps 324 and deforms to fill the voids around the bumps 324. Also, the adhesive film 326 bonds with the passivation surface 322 of the wafer 320.

Next, as shown in Fig. 9C, the wafer 320, which has been pre-coated with adhesive, is diced or divided into discrete integrated circuits 330. Finally, as shown in Fig. 9D, the backing layer 328 is removed from the integrated circuits 330 such that the adhesive layer 326 is exposed. With the backing 328 removed, the integrated circuits are ready for connection to a substrate.

It will be appreciated that other techniques could also be used to apply adhesive to the wafer. For example, the adhesive can be coated as a hot melt or coated from solution. Additionally, the above-described method can also include the step of removing portions of the adhesive from the bumps to generate exposed contact areas as previously disclosed in the detailed description.

With regard to the foregoing description, it is to be understood that changes may be made in detail, especially in matters of the construction materials employed and the shape, size, and arrangement of the parts without departing from the scope of the present invention. It is intended that the specification and depicted embodiment be considered exemplary only, with a true scope and spirit of the invention being indicated by the broad meaning of the following claims.

We claim:

1. A method for connecting an integrated circuit chip to a circuit substrate, the integrated circuit chip including a bumped side having a plurality of conductive bumps, the method comprising the steps of:

applying adhesive directly to the bumped side of integrated circuit chip;

removing portions of the adhesive to expose contact regions of the conductive bumps; and

pressing the bumped side of the integrated circuit chip against the circuit substrate such that the bumps provide an electrical connection between the integrated circuit chip and the circuit substrate, and the adhesive forms a bond between the integrated circuit chip and the circuit substrate.

2. The method of claim 1, wherein the adhesive is applied to the integrated circuit chip by a technique selected from the group of coating the adhesive as a hot melt, coating the adhesive from solution, bonding the adhesive as a film in a lamination process, and pressing the adhesive as a film onto the bumped side of the integrated circuit chip.

3. A method for manufacturing integrated circuit chips comprising the steps of:

providing a wafer including a bumped side having a plurality of conductive bumps;

applying adhesive to the bumped side of the wafer; and

dicing the wafer on which the adhesive has been applied into individual integrated circuit chips.

4. The method of claim 3, wherein the adhesive is applied to the wafer by a technique selected from the group of coating the adhesive as a hot melt, coating the

adhesive from solution, bonding the adhesive as a film in a lamination process, and pressing the adhesive as a film onto the bumped side of the wafer.

5. The method of claim 3, wherein when the adhesive is applied to the bumped side of the wafer, the conductive bumps are overcoated with adhesive.

6. The method of claim 5, wherein prior to dicing the wafer, overcoat portions of the adhesive are removed to expose contact regions of the conductive bumps.

7. The method of claim 6, wherein after removing the overcoat portions of the adhesive, the exposed contact regions of the conductive bumps are substantially flush with a primary exposed surface of the adhesive.

8. The method of claim 6, wherein after the overcoat portions of adhesive are removed, and prior to dicing the wafer, a protective cover is placed over the adhesive and exposed contact regions.

9. An integrated circuit chip comprising:

a bumped side having a passivation surface on which a plurality of conductive bumps are disposed; and

a layer of adhesive that covers the bumped side of the circuit substrate, the adhesive having an primary surface that is substantially parallel to the passivation surface, and the conductive bumps having exposed contact regions that are not covered by the adhesive.

10. The integrated circuit chip of claim 9, wherein the conductive bumps have heights approximately equal to or greater than a thickness of the adhesive.

11. The integrated circuit chip of claim 9, wherein the exposed contact regions of the conductive bumps are substantially flush with the primary surface of the adhesive.

12. The integrated circuit chip of claim 9, wherein portions of the conductive bumps project outward from the primary surface of the adhesive such that a stand off exists between the exposed contact regions of the conductive bumps and the primary surface of the adhesive.

13. A conductive tape comprising:

an adhesive layer having a top surface and a bottom surface; and

a plurality of conductive particles disposed within the adhesive layer, at least one of the particles having an exposed top contact region at the top surface of the adhesive layer, and an exposed bottom contact region at the bottom surface of the adhesive layer.

14. The conductive tape of claim 13, wherein the top contact region of the at least one particle is substantially flush with the top surface of the adhesive layer.

15. The conductive tape of claim 14, wherein the bottom contact region of the at least one particle is substantially flush with the bottom surface of the adhesive layer.

16. A method for providing an electrical connection between first and second electrical components comprising:

providing a conductive tape having an adhesive layer including a top surface opposite a bottom surface and a plurality of conductive particles disposed within the adhesive layer, extending across a thickness of the

adhesive layer, and including an exposed top contact region located at the top surface of the adhesive layer and an exposed bottom contact region located at the bottom surface of the adhesive layer; and

pressing the conductive tape between the first and second electrical components.

17. The method of claim 16, further comprising the step of heating the conductive tape either while the conductive tape is pressed between the first and second electrical components or after the conductive tape is pressed between the first and second electrical components.

18. A method for making a conductive tape comprising the steps of:

providing an adhesive layer containing conductive particles; and

removing portions of the adhesive that overcoat the conductive particles such that exposed contact regions of the conductive particles are generated.

19. The method of claim 18, wherein the portions of adhesive that overcoat the conductive particles are removed by abrasion.

20. The method of claim 18, wherein prior to the removing step, the conductive particles are larger than a thickness of the adhesive.

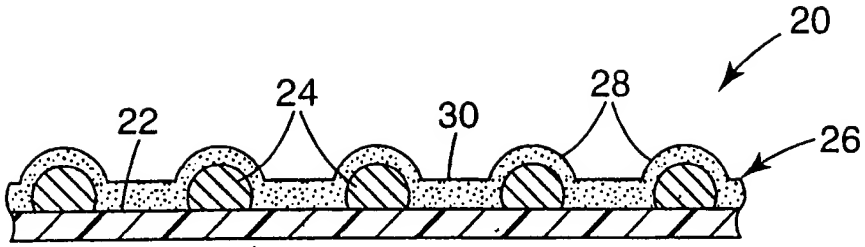

Fig. 1A

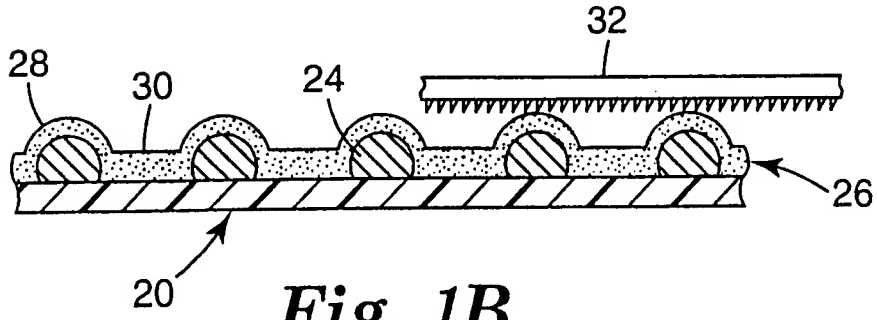

Fig. 1B

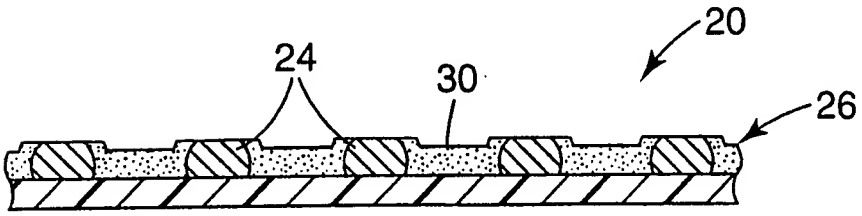

Fig. 1C

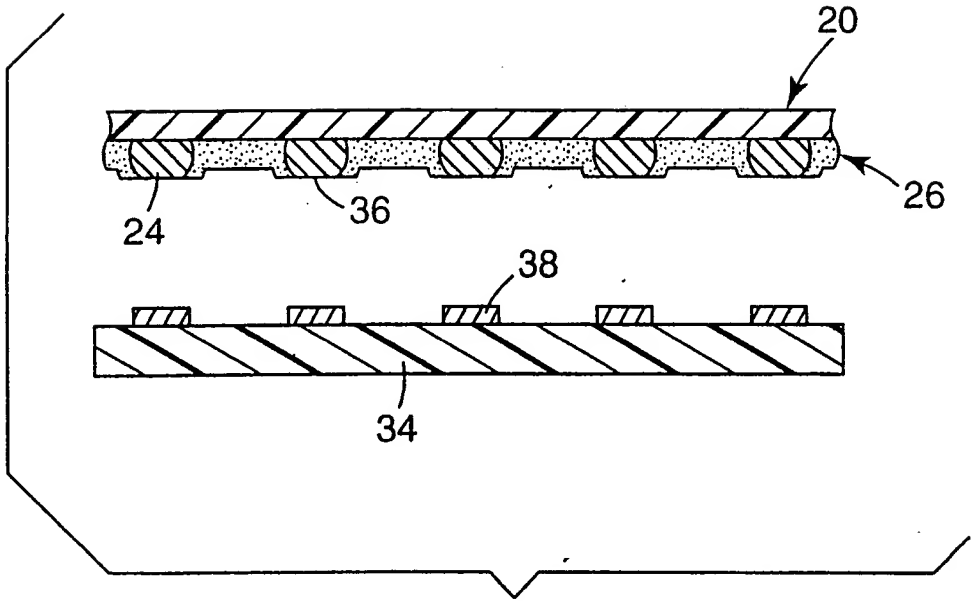

Fig. 2A

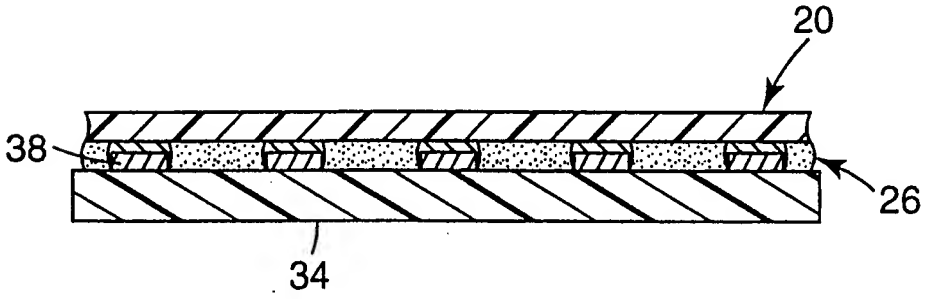

Fig. 2B

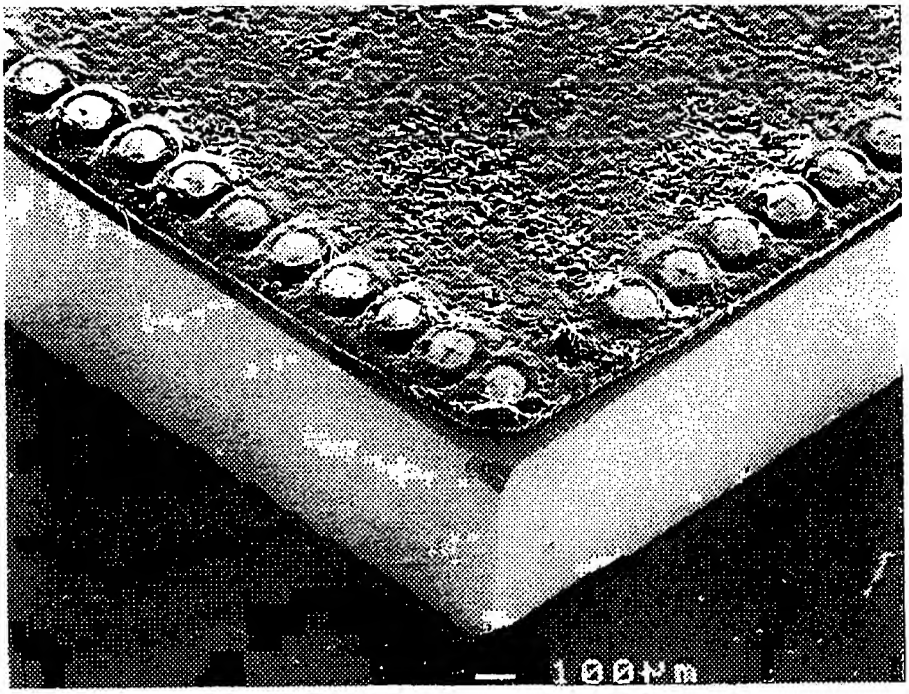

FIG.3A

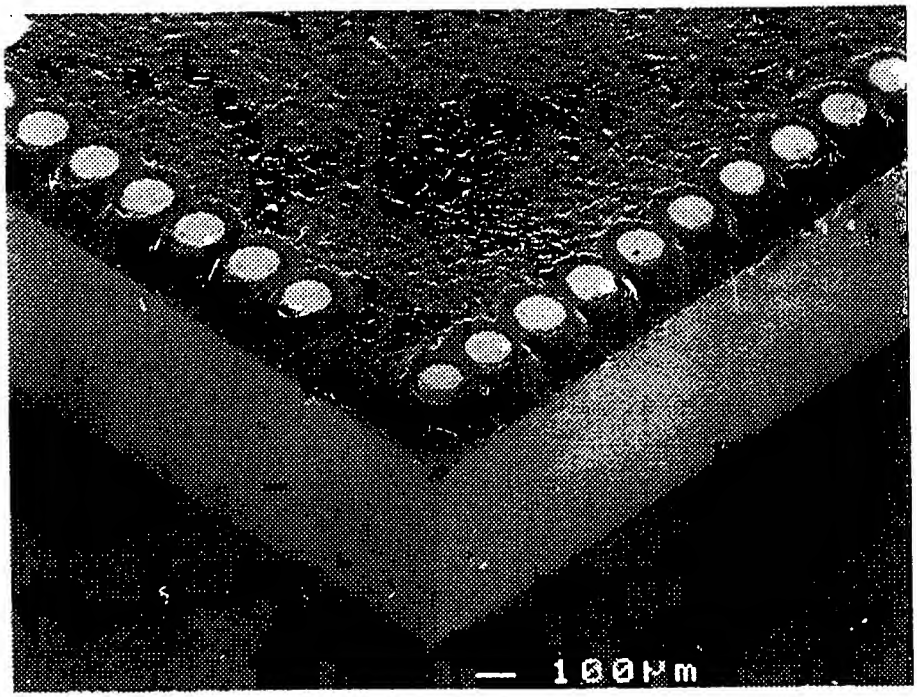

FIG.3B

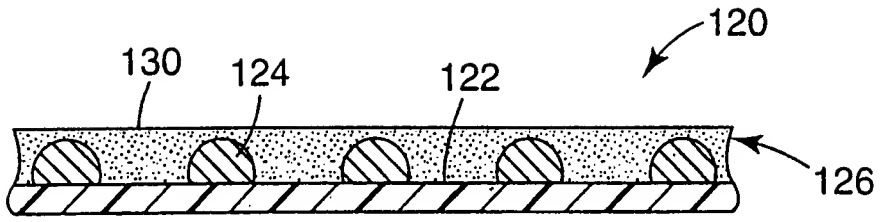

Fig. 4A

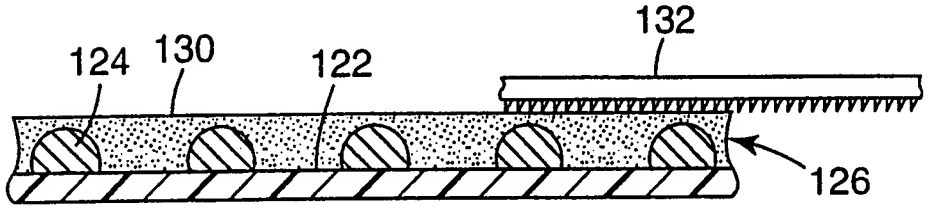

Fig. 4B

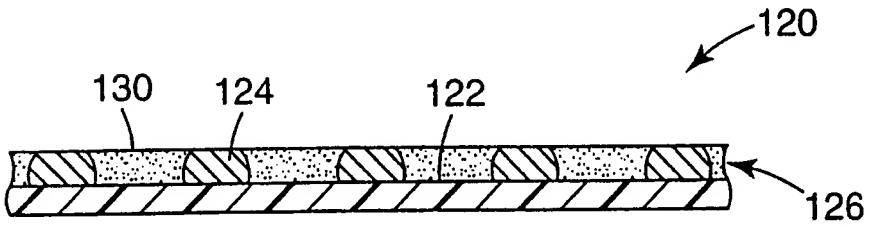

Fig. 4C

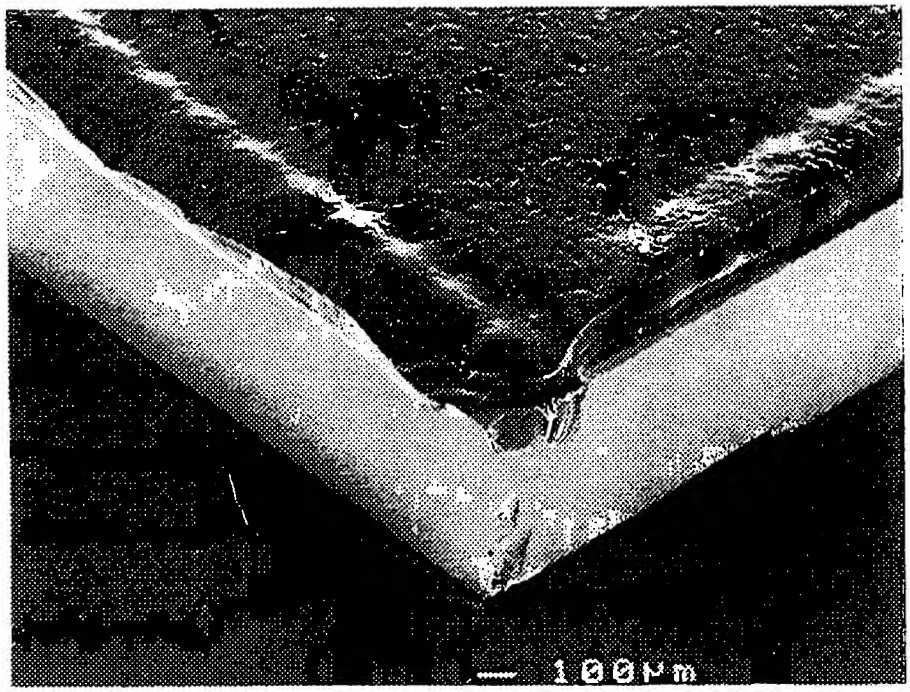

FIG.5A

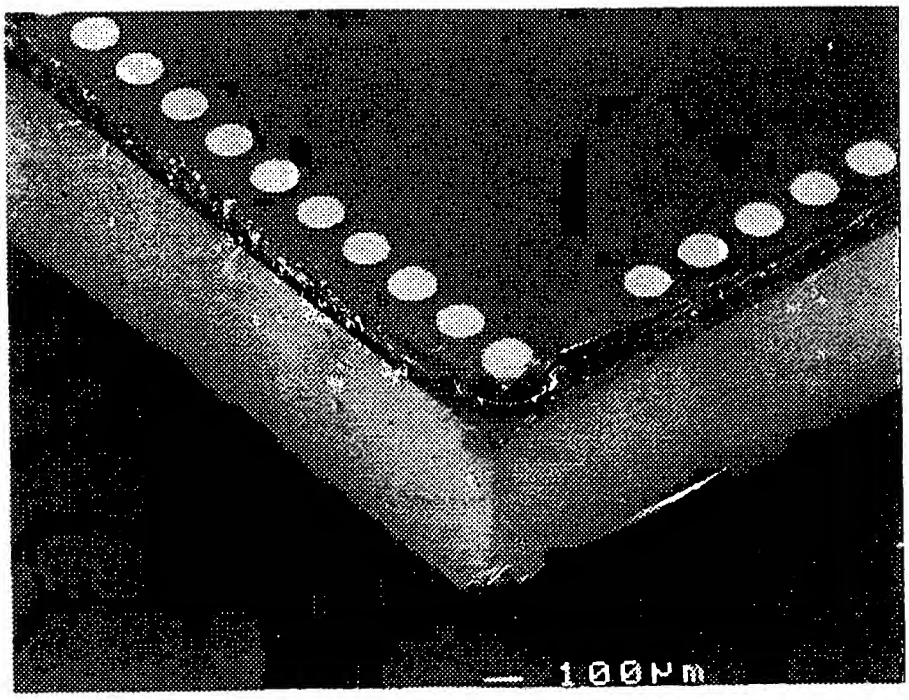

FIG.5B

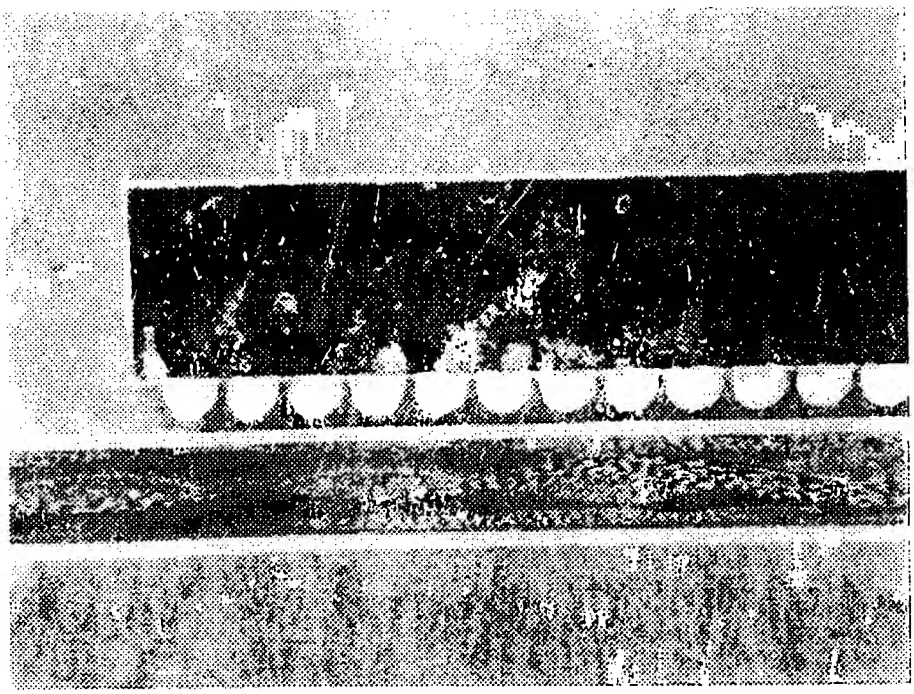

FIG.6A

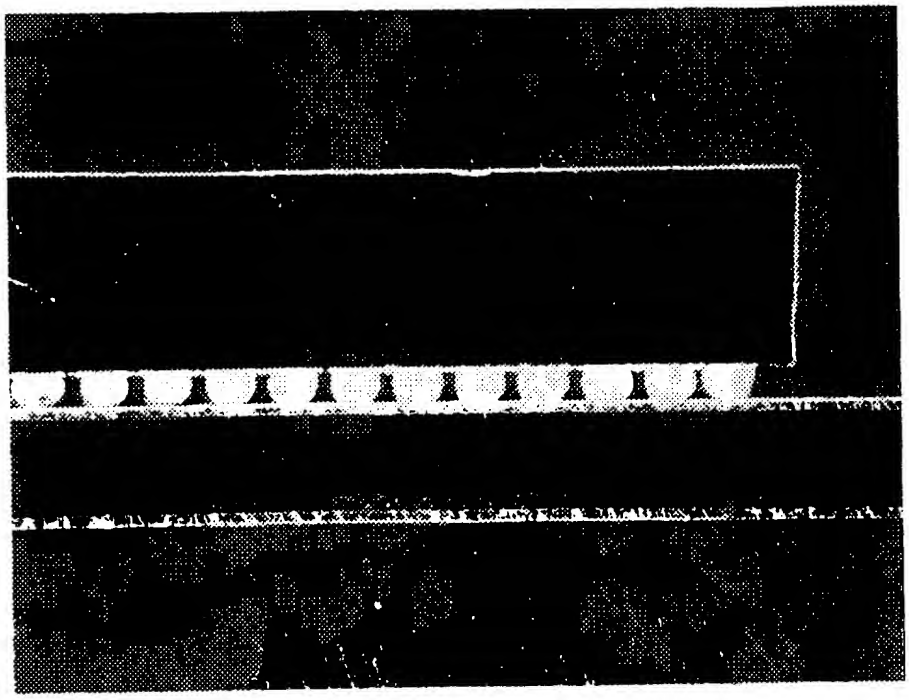

FIG.6B

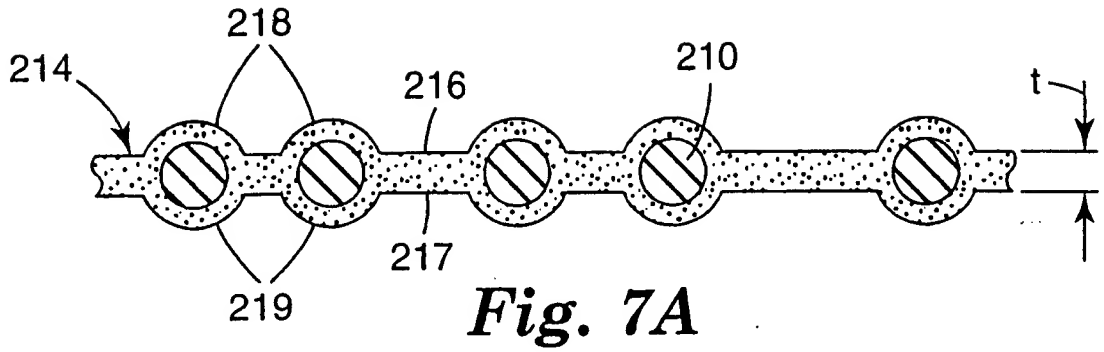

Fig. 7A

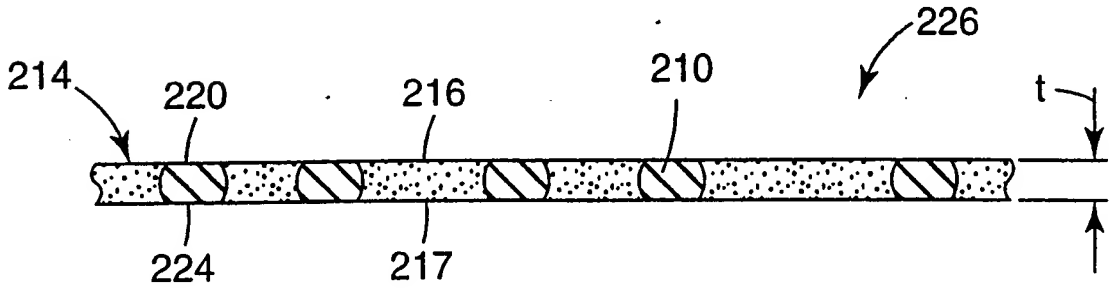

Fig. 7B

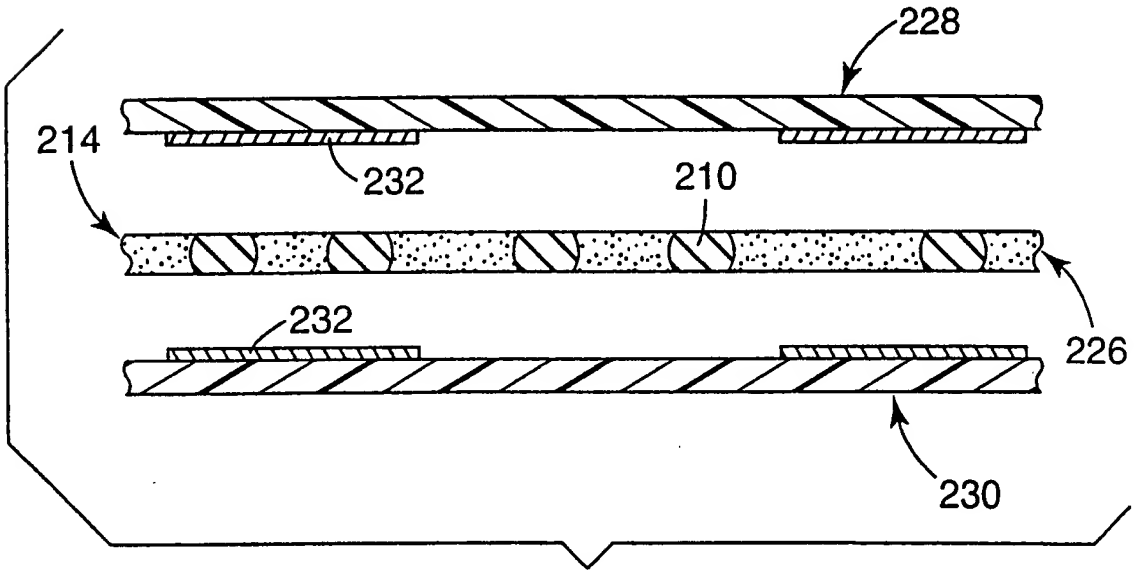

Fig. 8A

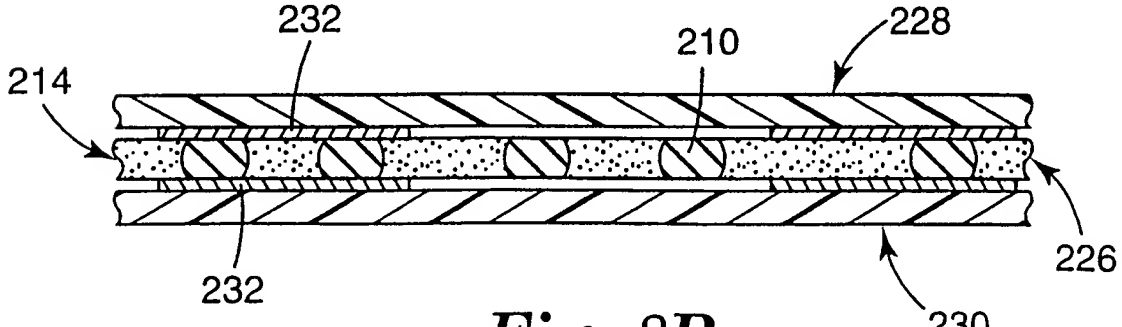

Fig. 8B

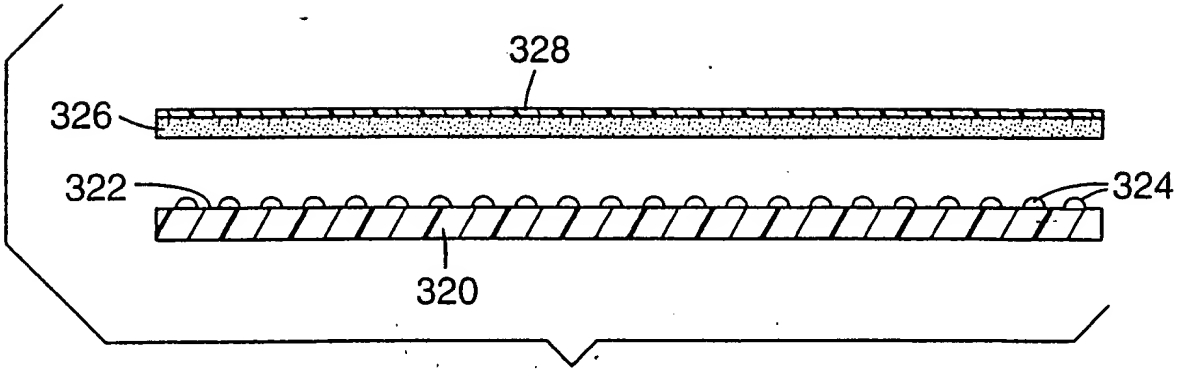

Fig. 9A

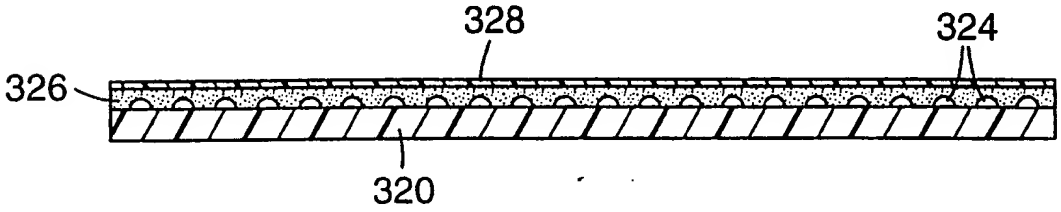

Fig. 9B

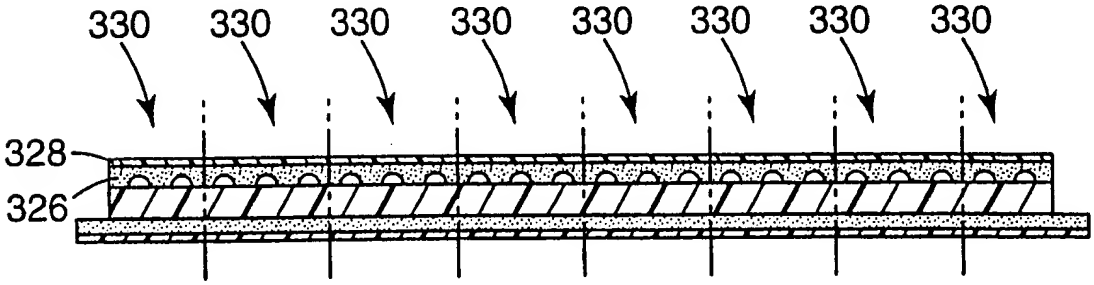

Fig. 9C

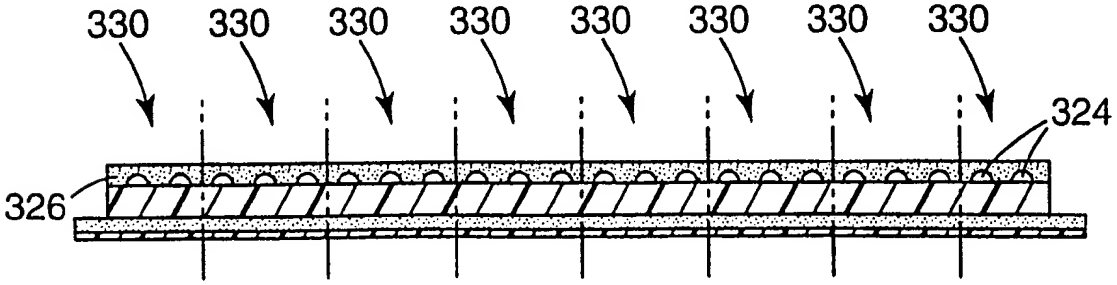

Fig. 9D

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/56 H01L21/48

According to International Patent Classification(IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 543 585 A (BOOTH RICHARD B ET AL) 6 August 1996	1,9
A	see column 2, line 47 - line 62; figures 3,9,14 see column 3, line 49 - line 60	3,5,7, 10-12
X	DE 40 08 624 A (BOSCH GMBH ROBERT) 11 October 1990	1,9
A	see column 4, paragraph 3 - column 5, paragraph 4; figure 4	2,4,12
X	EP 0 560 072 A (NITTO DENKO CORP) 15 September 1993	13
A	see claim 1	20

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publicationdate of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of theinternational search	Date of mailing of the international search report
18 August 1998	25/08/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	De Raeve, R

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Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GILLEO K: "DIRECT CHIP INTERCONNECT USING POLYMER BONDING" PROCEEDINGS OF THE ELECTRONIC COMPONENTS CONFERENCE, HOUSTON, MAY 22 - 24, 1989, no. CONF. 39, 22 May 1989, pages 37-44, XP000123782 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS see figure 5 ---	13,16
A	EP 0 332 402 A (SHARP KK) 13 September 1989 see column 11, line 57 - column 12, line 26; figures 15,16 ---	1,13,16
A	"DIRECT CHIP BOMDING USING TRANSFERRED CONDUCTIVE ADHESIVE FILM" IBM TECHNICAL DISCLOSURE BULLETIN, vol. 32, no. 10B, 1 March 1990, page 474/475 XP000097963 -----	

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5543585 A	06-08-1996	JP 2596721 B	02-04-1997
		JP 7231011 A	29-08-1995
		US 5747101 A	05-05-1998
DE 4008624 A	11-10-1990	JP 3018040 A	25-01-1991
		US 5068714 A	26-11-1991
EP 0560072 A	15-09-1993	JP 5258789 A	08-10-1993
		JP 5258790 A	08-10-1993
		US 5438223 A	01-08-1995
EP 0332402 A	13-09-1989	JP 1227444 A	11-09-1989
		JP 2596960 B	02-04-1997
		US 4963002 A	16-10-1990

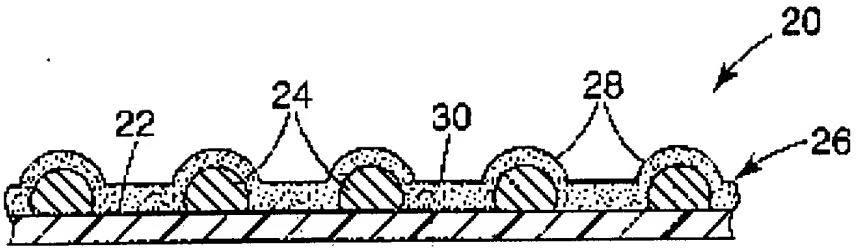

Fig. 1A

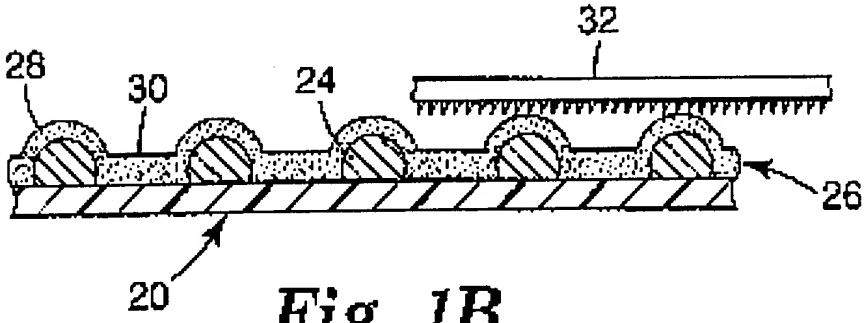

Fig. 1B

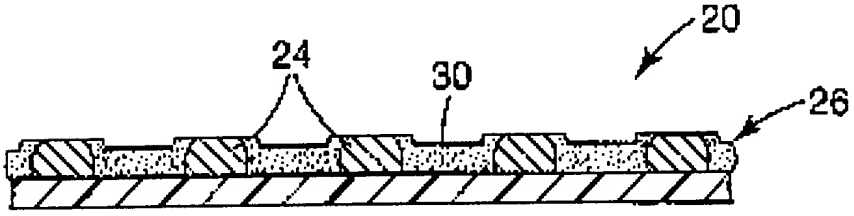

Fig. 1C

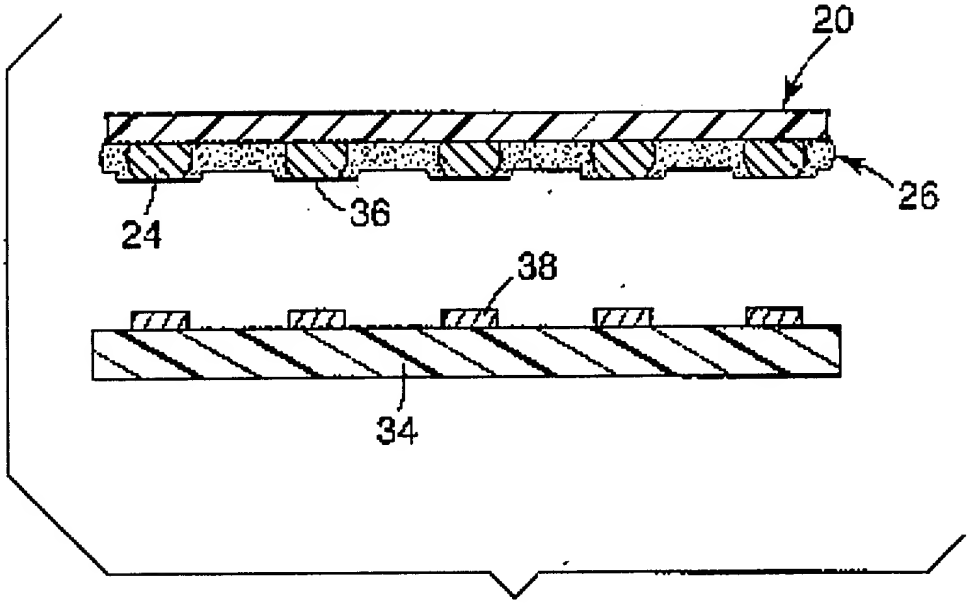

Fig. 2A

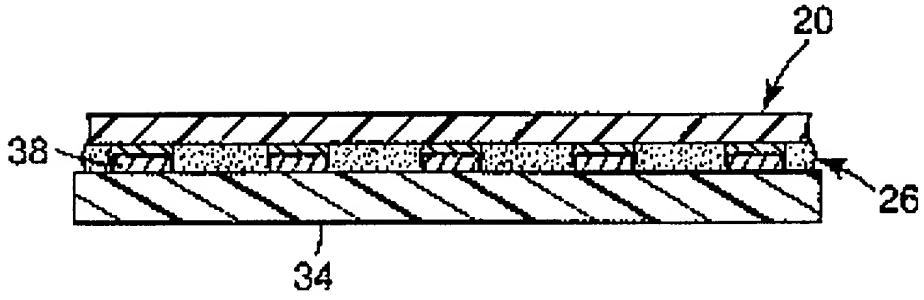

Fig. 2B

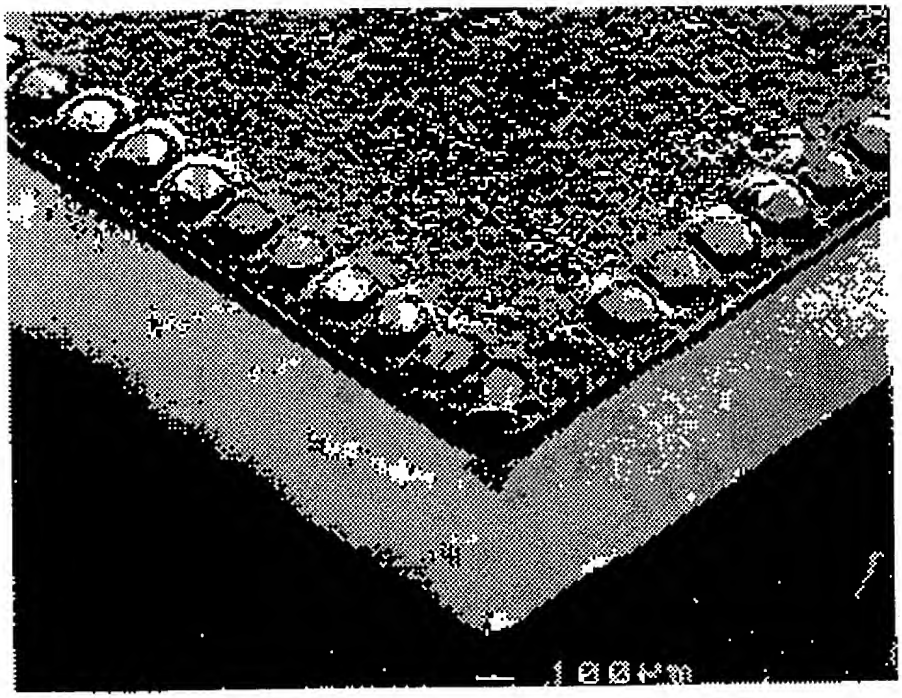

FIG.3A

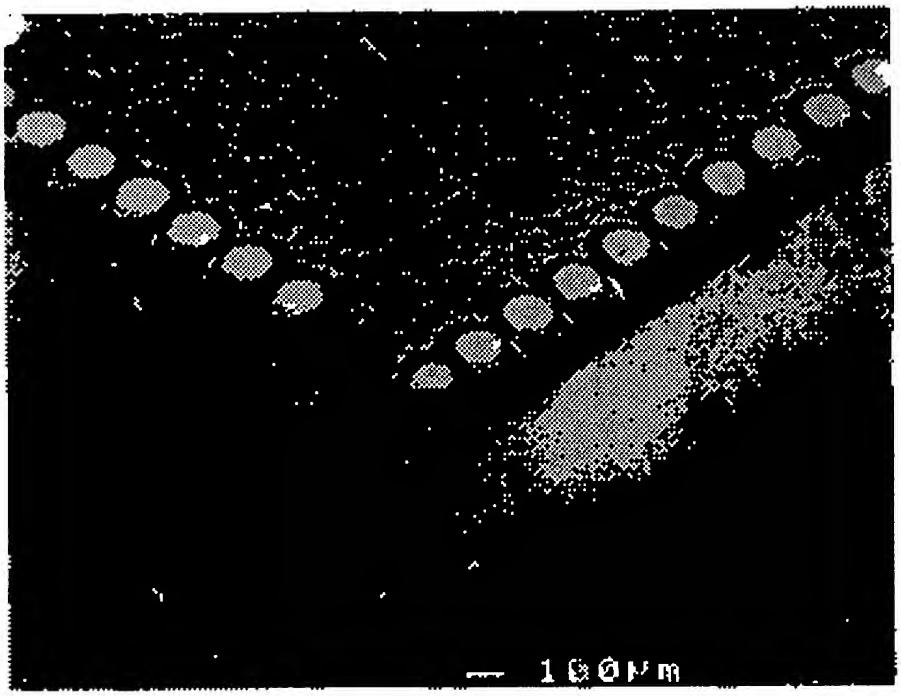

FIG.3B

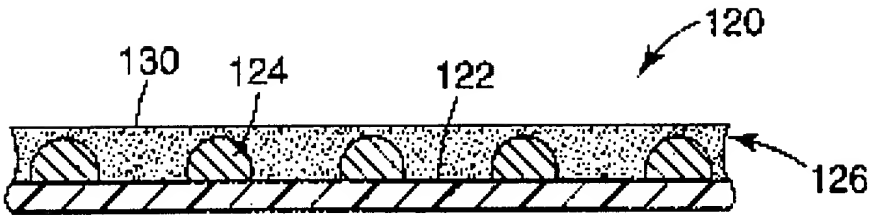

Fig. 4A

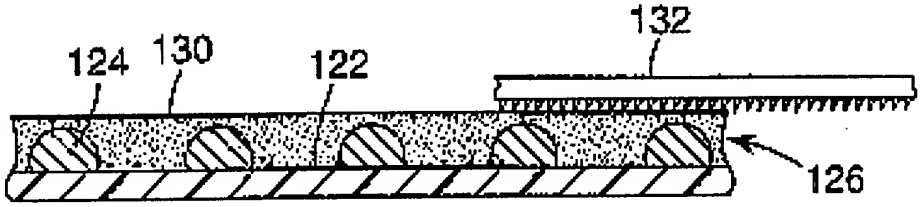

Fig. 4B

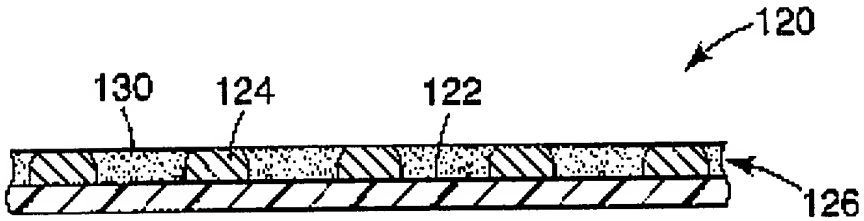

Fig. 4C

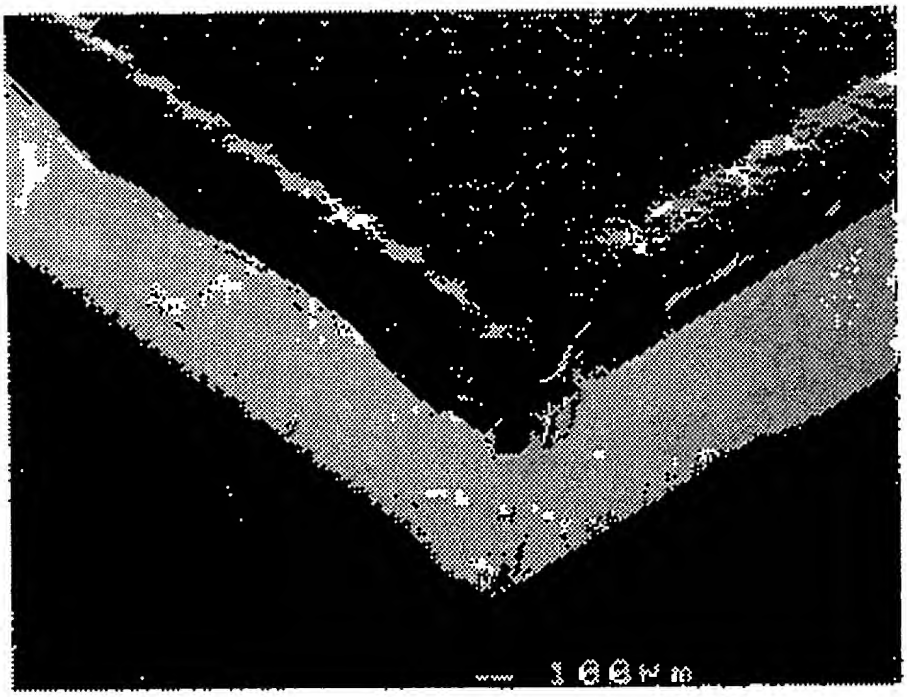

FIG.5A

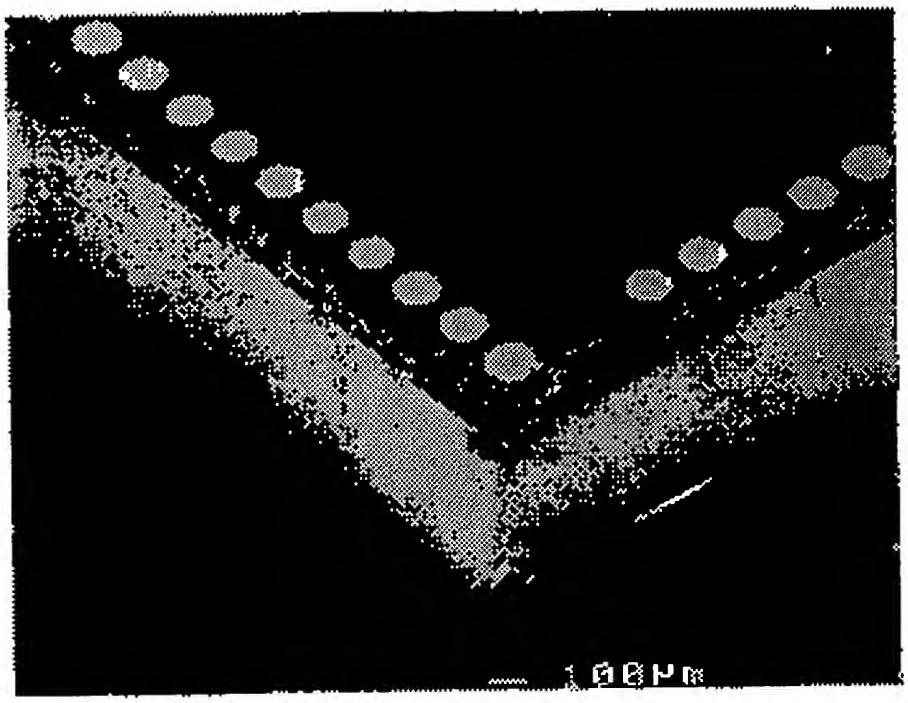

FIG.5B

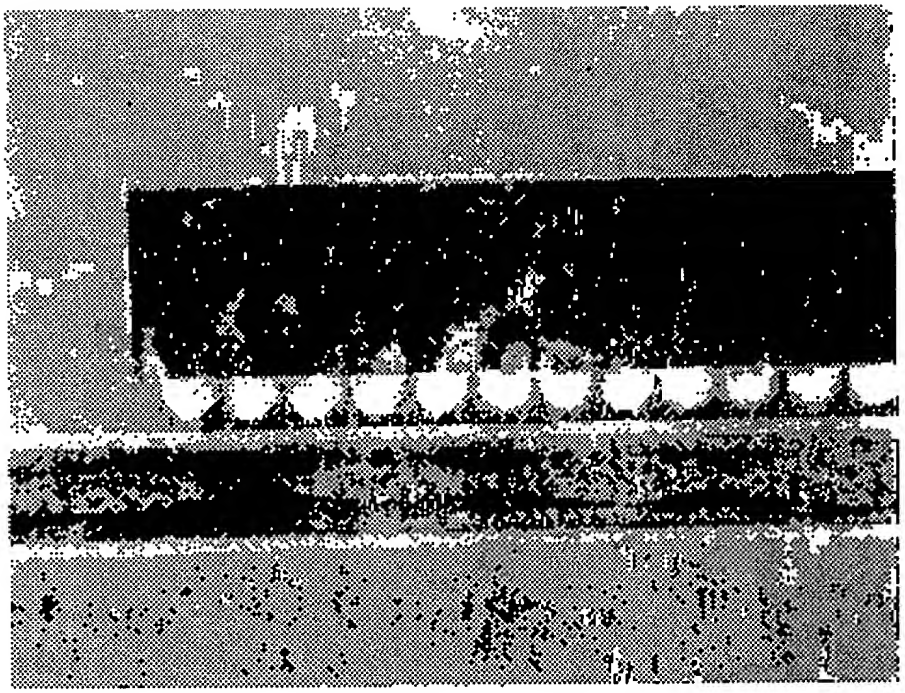

FIG.6A

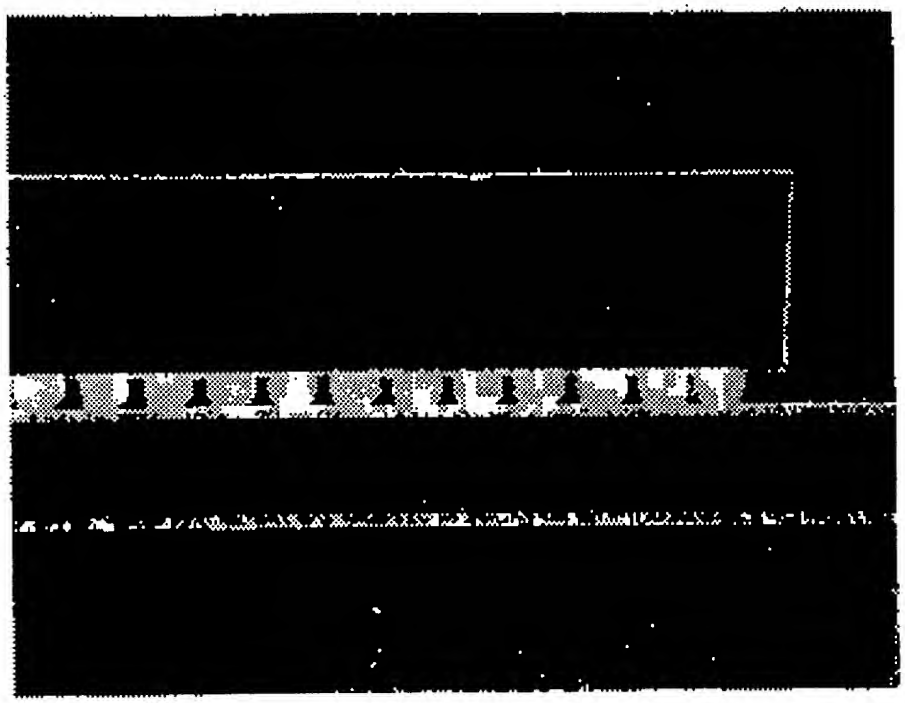

FIG.6B

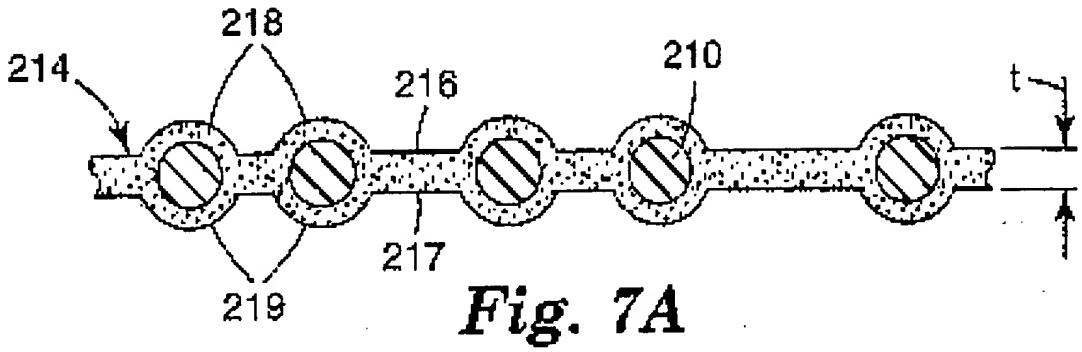

Fig. 7A

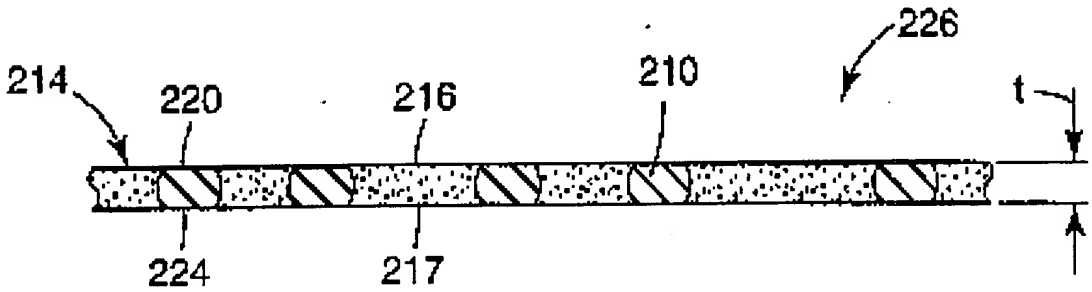

Fig. 7B

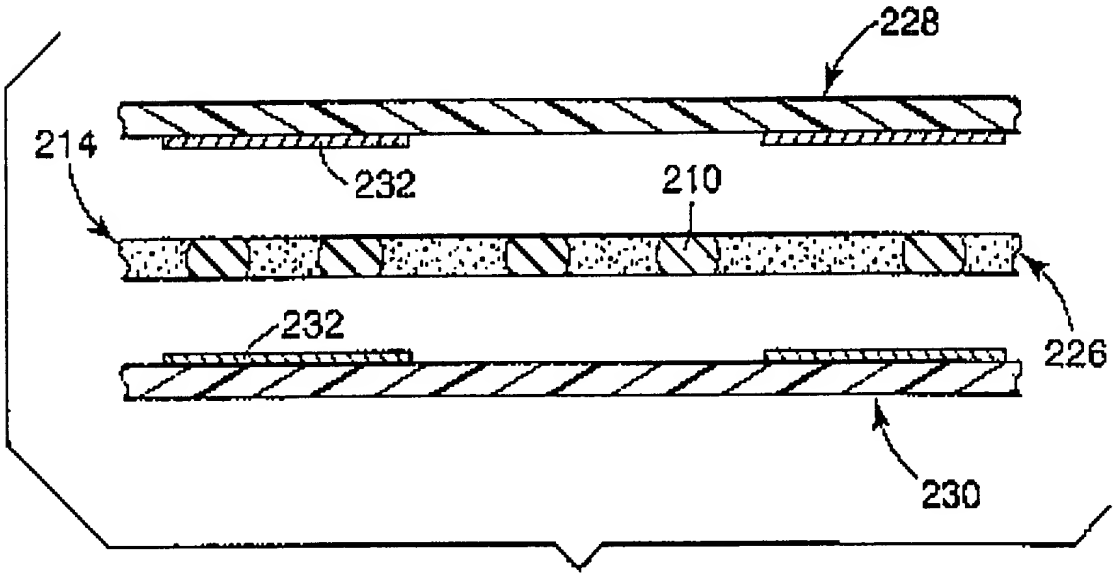

Fig. 8A

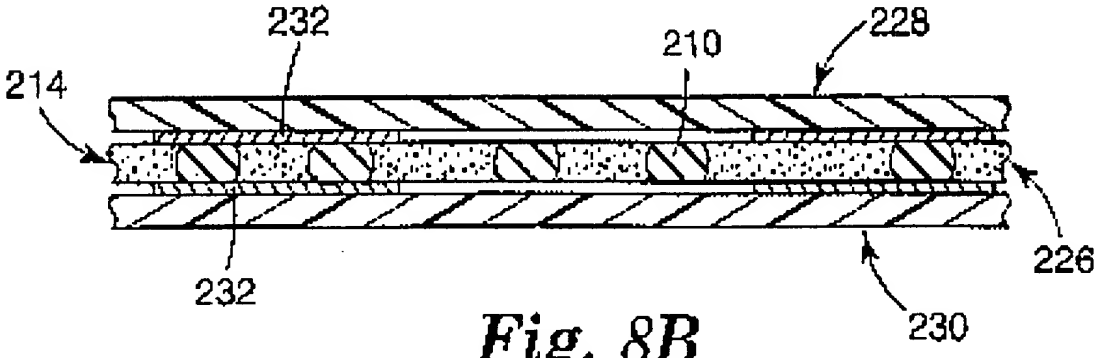

Fig. 8B

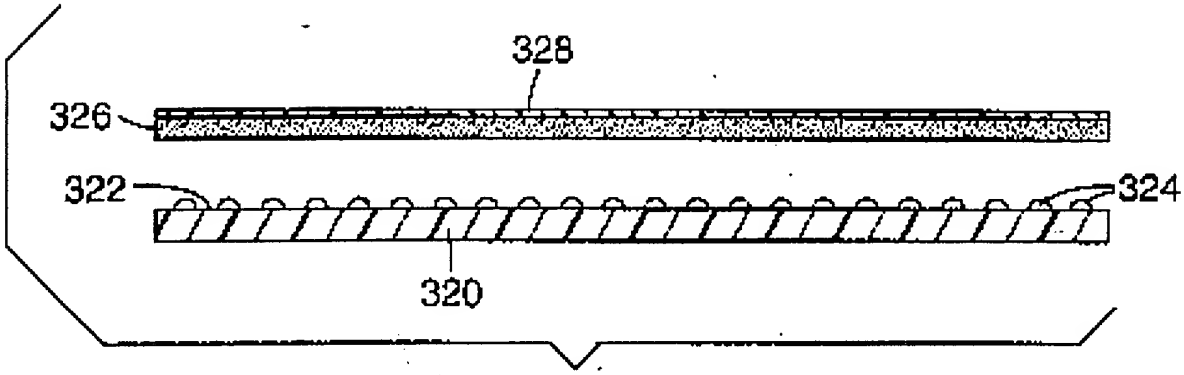

Fig. 9A

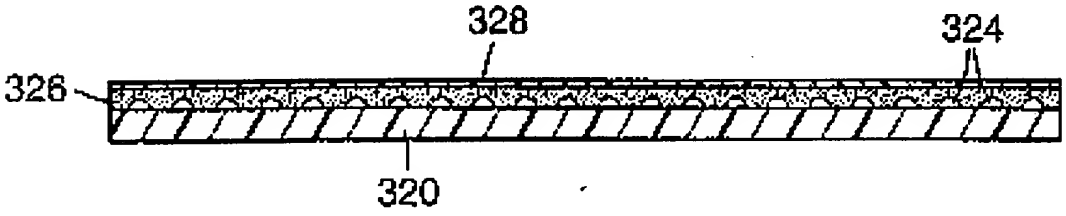

Fig. 9B

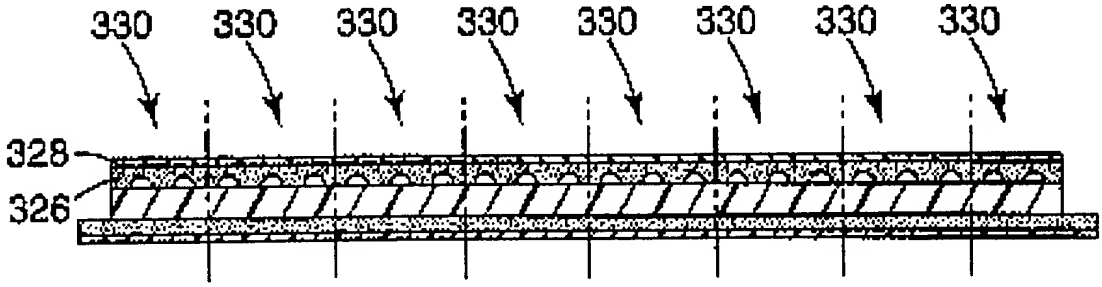

Fig. 9C

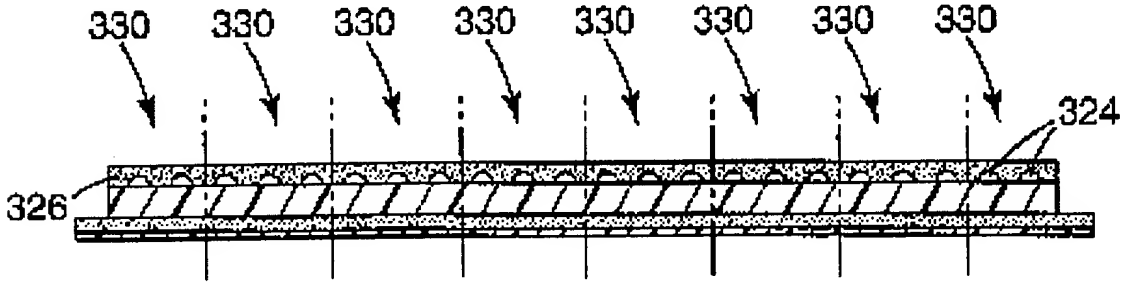

Fig. 9D